Logic Design – Lab 3: "Design of asynchronous sequential logic circuits using transition tables and output tables" - suplement

a

x_2	0	0	1	0	0	0	1	0	1	0	0	0	0	
x_1	0	1	1	0	0	1	1	1	1	1	0	1	0	
$y=(y_1 y_2)$	00	10	11	01	00	10	11	01	11	10	00	01	00	
A	1	2	4	3	1	2	4	3	5	2	0	3	1	

b

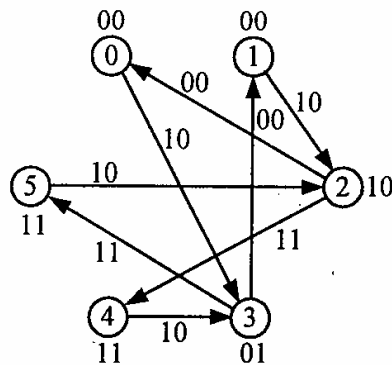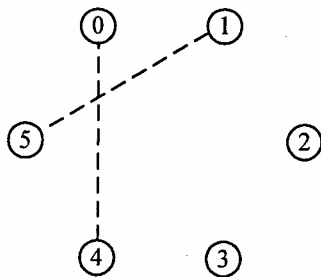| A^t \ $x_1 x_2$	00	01	11	10	$y_1 y_2$
0	(0)	–	–	3	00
1	(1)	–	–	2	00
2	0	–	4	(2)	10
3	1	–	5	(3)	01
4	–	–	(4)	3	11
5	–	–	(5)	2	11

A^{t+1}

c

Fig. 1. Time diagram (a), transition table and output map (b), design graph of given asynchronous sequential logic circuit (c).

a

b

	0	1	2	3	4
1	2,3				
2	2,3	0,1			
3	0,1	2,3	X		
4	B 2,3	2,3	4,5		
5	2,3	B 4,5	2,3	2,3	

c

A^t \ $x_1 x_2$	00	01	11	10
0,4	(0)	–	(4)	3
1,5	(1)	–	(5)	2
2	0	–	4	(2)
3	1	–	5	(3)

A^{t+1}

d

A^t \ $x_1 x_2$	00	01	11	10
0	(0)	–	(0)	3
1	(1)	–	(1)	2
2	0	–	0	(2)
3	1	–	1	(3)

A^{t+1}

e

A^t \ $x_1 x_2$	00	01	11	10
0	00	--	11	01
1	00	--	11	10
2	-0	--	1-	10
3	0-	--	-1	01

$y^t = (y_1 y_2)$

Fig. 2. Reducing transition table: transition table with original state numbering (c) and with new internal state numbering (d), output table – for Mealy type automata (e).

a

```
      00            01
     (0) ─────────▶(3)
      │             │
      │             │
      ▼             ▼
     (2)◀───────── (1)
      10            11
```

b

$Q_1'Q_2'$ \ x_1x_2	00	01	11	10
(0) 00	00	--	00	01
(3) 01	11	--	11	01
(1) 11	11	--	11	10
(2) 10	00	--	00	10

$$Q_1'^{t+1}Q_2'^{t+1}$$

c

$Q_1'Q_2'$ \ x_1x_2	00	01	11	10
00	00	--	11	01
01	0-	--	-1	01
11	00	--	11	10
10	-0	--	1-	10

$$y' = (y_1 y_2)$$

d

$Q_1'Q_2'$ \ x_1x_2	00	01	11	10
00	0	–	0	0
01	1	–	1	0
11	1	–	1	1
10	0	–	0	1

$$Q_1^{t+1}$$

$Q_1'Q_2'$ \ x_1x_2	00	01	11	10
00	0	–	0	1
01	1	–	1	1
11	1	–	1	0
10	0	–	0	0

$$Q_2^{t+1}$$

e

$Q_1'Q_2'$ \ x_1x_2	00	01	11	10
00	0	–	1	0
01	0	–	–	0
11	0	–	1	1
10	–	–	1	1

$$y_1^t$$

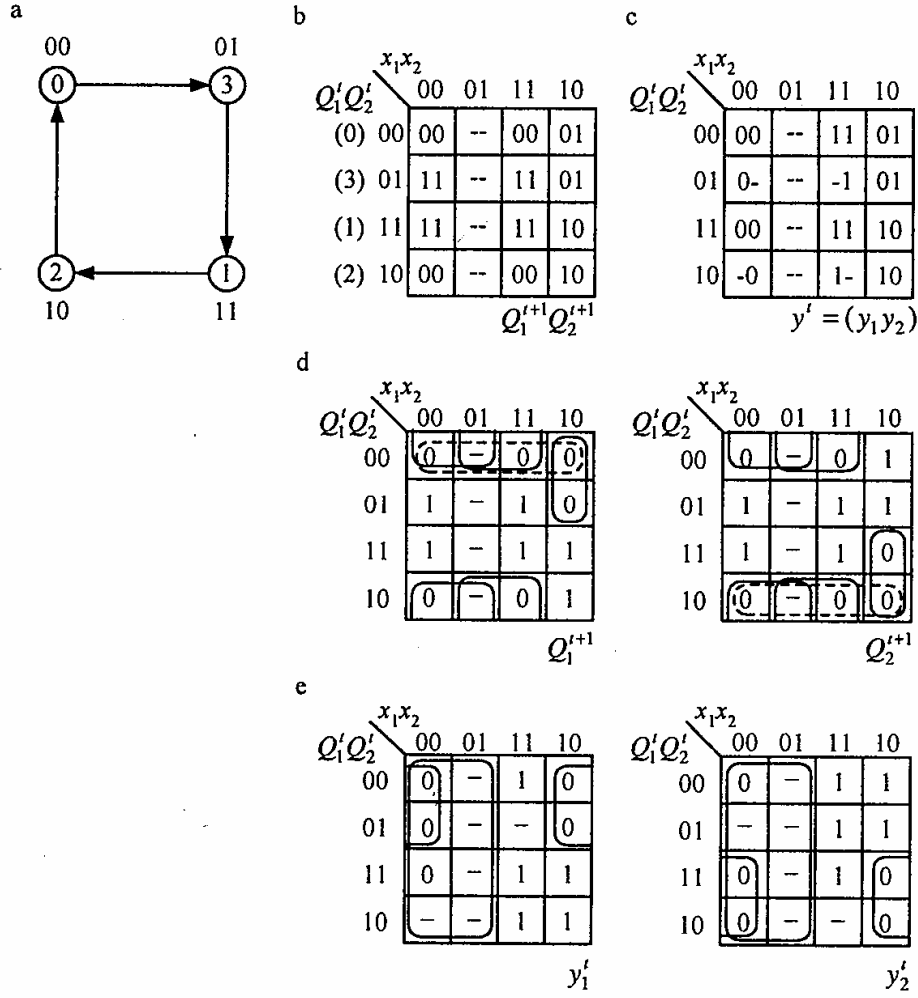| $Q_1'Q_2'$ \ x_1x_2	00	01	11	10
00	0	–	1	1
01	–	–	1	1
11	0	–	1	0
10	0	–	–	0

$$y_2^t$$

Fig. 3. Internal states encoding: encoded transition table (b), encode output table (c), Karnaugh maps for internal states: Q_1 and Q_2 (d), Karnaugh maps for both outputs y_1 and y_2 (e).

$$Q_1^{t+1} = (Q_2^t + x_1)(Q_2^t + \bar{x}_2)(Q_1^t + Q_2^t)(\bar{x}_1 + x_2 + Q_1^t),$$

$$Q_2^{t+1} = (Q_2^t + x_1)(Q_2^t + \bar{x}_2)(\overline{Q}_1^t + Q_2^t)(\bar{x}_1 + x_2 + \overline{Q}_1^t),$$

$$y_1^t = x_1(Q_1^t + x_2),$$

$$y_2^t = x_1(\overline{Q}_1^t + x_2).$$

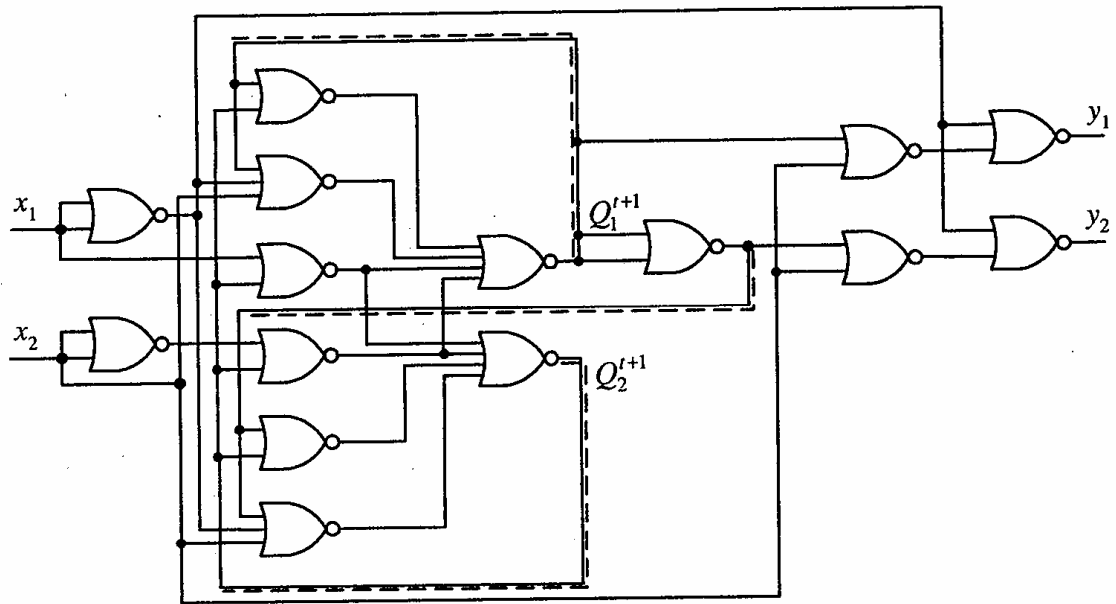Fig. 4. Boolean functions of Q_1, Q_2, y_1 and y_2.

Fig. 5. Circuit with NOR gates.

Implementation with S-R flip flops:

a

$Q_1^t Q_2^t$ \ $x_1 x_2$	00	01	11	10
(0) 00	0	–	0	0
(3) 01	1	–	1	0
(1) 11	1	–	1	1
(2) 10	0	–	0	1

Q_1^{t+1}

$Q_1^t Q_2^t$ \ $x_1 x_2$	00	01	11	10
00	0	–	0	1
01	1	–	1	1
11	1	–	1	0
10	0	–	0	0

Q_2^{t+1}

b

$Q_1^t \to Q_1^{t+1}$		s r
0	0	0 –
0	1	1 0
1	0	0 1
1	1	– 0

$Q_1^t Q_2^t$ \ $x_1 x_2$	00	01	11	10
00	0-	--	0-	0-
01	10	--	10	0-
11	-0	--	-0	-0
10	01	--	01	-0

$s_1 r_1$

$Q_1^t Q_2^t$ \ $x_1 x_2$	00	01	11	10
00	0-	--	0-	10
01	-0	--	-0	-0
11	-0	--	-0	01
10	0-	--	0-	0-

$s_2 r_2$

c

$Q_1^t Q_2^t$ \ $x_1 x_2$	00	01	11	10
(0) 00	0	–	0	0
(3) 01	1	–	1	0
(1) 11	–	–	–	–
(2) 10	0	–	0	–

s_1

	00	01	11	10
	–	–	–	–
	0	–	0	–
	0	–	0	0
	1	–	1	0

r_1

	00	01	11	10
	0	–	0	1
	–	–	–	–
	–	–	–	0
	0	–	0	0

s_2

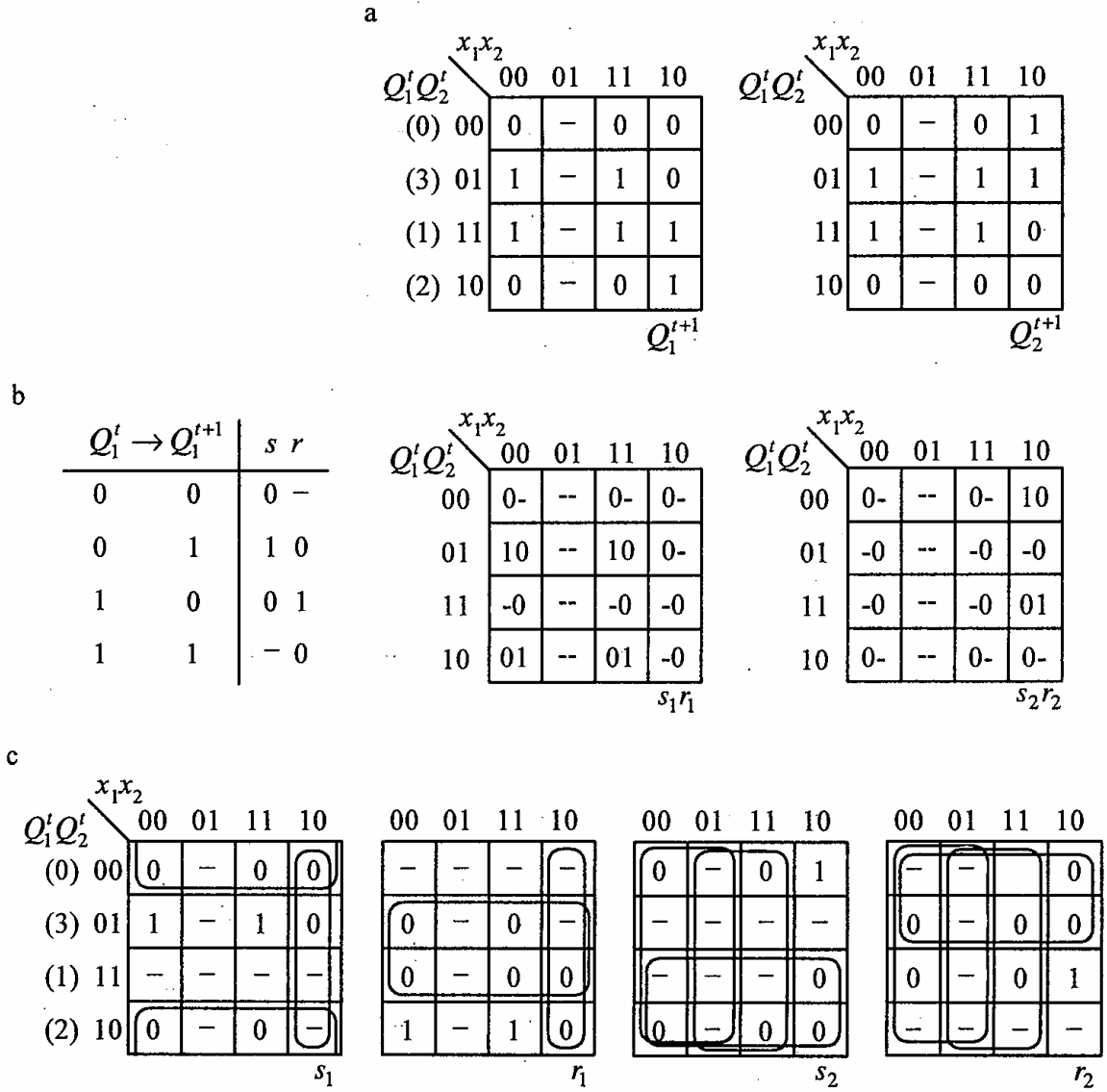|	00	01	11	10
	–	–	–	0
	0	–	0	0
	0	–	0	1
	–	–	–	–

r_2

Fig. 6. Excitation functions of "memory": encoded transition tables (a), excitation table of S-R latch (Set-Reset flip-flop), separated excitation tables for S-R inputs (c).

$$s_1 = Q_2^t(\overline{x_1} + \overline{x_2}), \quad r_1 = \bar{Q}_2^t(\overline{x_1} + x_2), \quad s_2 = \bar{Q}_1^t x_1 \overline{x_2}, \quad r_2 = Q_1^t x_1 \overline{x_2}$$

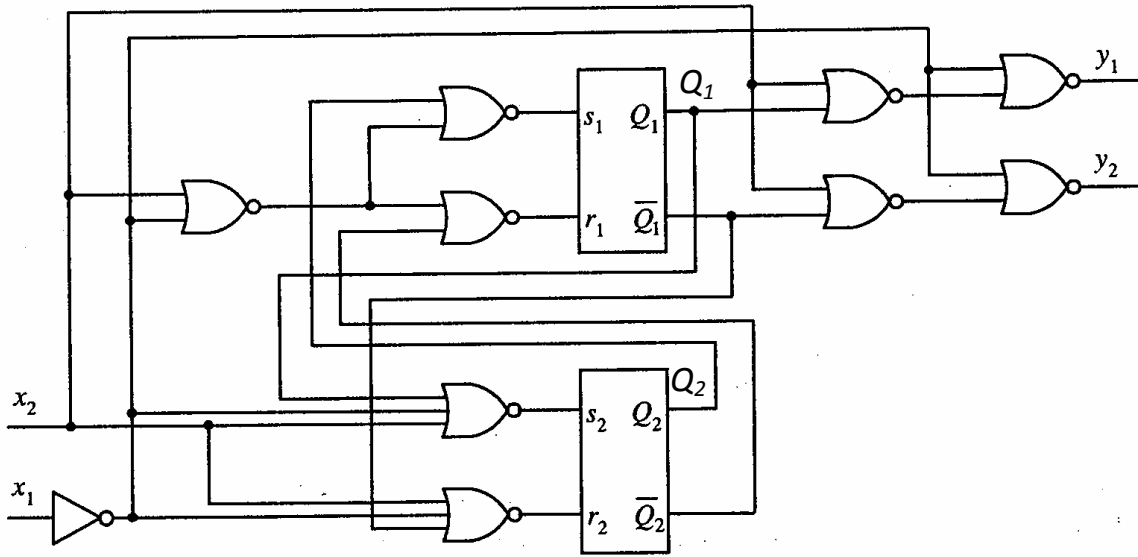Fig. 7. Boolean functions of s_1, r_1, ys_2 and r_2.

4

Fig. 8. Circuit with S-R flip-flops as internal states Q_1 and Q_2 memory elements.